EFFECT OF EXTENDED DEFECTS ON THE ELECTRICAL PROPERTIES OF COMPENSATED SOLAR GRADE MULTICRYSTALLINE SILICON

J. Libal[*], M. Acciarri[*], S. Binetti[*], R. Kopecek[Δ], R. Petres[Δ], C. Knopf[+], K. Wambach[+]

[*]University of Milano Bicocca, Dipartimento di Scienza dei Materiali Università degli Studi Milano-Bicocca, via Cozzi 53, I-20125 Milano, Italy, joris.libal@unimib.it

[Δ]ISC-Konstanz, Rudolf-Diesel-Str. 15, D-78467 Konstanz, Germany

[+]Deutsche Solar AG, Alfred-Lange Str. 18, D-09599 Freiberg/Sachsen, Germany

ABSTRACT: The current reduced availability and the high cost of electronic grade silicon for solar cell application pushed the photovoltaic industry towards faster development and alternative innovations: on one side the processing of thinner wafers and on the other, the production of low cost material with lower purity, the so called “solar grade silicon” (SoG-Si, e.g. [1]). The use of this material in solar cell production depends strongly on the possible improvement of the electronic quality during the solar cell process and requires a better knowledge of the interaction of the impurities with extended defects. In addition to a higher concentration of metallic and other impurities, some SoG-Si production techniques will contain a high amount of dopants [2] and thus require compensation to obtain Si wafers with a resistivity compatible for solar cell production. This article presents a study of three p-type mc-Si ingots with different levels of compensation – one of them featuring an overcompensated part and thus, allowing the study of compensated n-type mc-Si material. The electrical characteristics of the material are determined by measuring the minority charge carrier lifetime and the Hall-mobility at room-temperature. In addition, correlations between the local lifetime and the recombination activity of extended crystal defects are studied by temperature-dependent EBIC-measurements.

Keywords: Multicrystalline Silicon, Defects, Lifetime

1 INTRODUCTION

The use of n-type Si as well as the use of compensated Si for solar cell production could enlarge the choice of available Si material and thus facilitate the use of SoG-Si feedstock and consequently support the strong growth of the solar cell production capacities. The study of the electrical properties of n-type mc-Si has been subject of many studies in the recent years (e.g. [3,4,5,6]). The present work concentrates on the effects of compensation. Compensation by addition e.g. of boron or phosphorous to the feedstock of an mc-Si ingot can be necessary to reach the desired resistivity range. This article presents a study of three mc-Si ingots with different levels of compensation. All the three are grown from off-cut Si from industrial mc-Si ingots. The aim of this experimental study is to obtain information about the impact of compensation on the electrical quality of the material and thus on its usability for solar cell production. In addition, n-type samples from one region of the ingot with the highest level of compensation are measured and the results are compared with p-type samples from the same brick.

2 MATERIAL PROPERTIES

Three 240 kg p-type mc-Si ingots, grown in the same HEM furnace at *Deutsche Solar* from off-cut-Si taken from other mc-Si ingots: one uncompensated ingot with standard resistivity as a reference (F1), a second one with compensation (F2) and a third one with stronger compensation containing an overcompensated n-type region (F3). The use of Si off-cuts as feedstock causes a relatively high impurity concentration in all the ingots, similar to SoG-Si.

2.1 Resistivity profiles

The resistivity distribution along the ingot (measured on bricks in the center of the ingot using the 4-point-probe-technique) is shown for ingot F1 and F2 in Fig. 1. The uncompensated ingot shows the typical trend caused by the segregation of the dopant atoms (boron) and leading to a decrease of the resistivity towards at the top of the ingot. Due to its higher segregation coefficient, the phosphorous, which has been added to ingot F2, compensates the boron mostly at the top of the ingot, leading to an increase of the resistivity towards the top of the ingot.

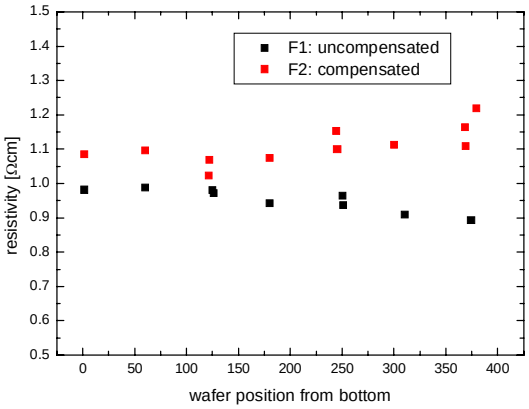


Figure 1: Resistivity profile of F1 (uncompensated) and F2 (compensated)

The resistivity profile of a corner brick from ingot F3, in which, compared to ingot F2, more phosphorous-doped material has been added for compensation, is shown in Fig. 2.

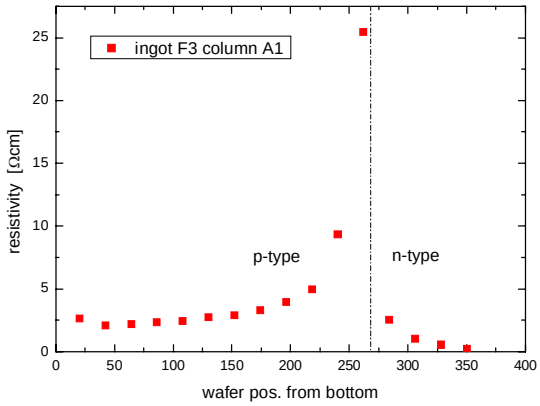


Figure 2: Resistivity profile of F3 (strongly compensated), column A1 (brick from the corner of the ingot)

2.2 As grown lifetime along the ingot heights

The minority charge carrier lifetimes have been measured by the microwave-detected PhotoConductance Decay technique (μW-PCD), the surfaces being passivated by a SiN_x-film, created by Plasma enhanced Chemical Vapour Deposition (PECVD). The evolution of the lifetime along the ingot height of the as grown wafers is shown for F1, F2 and F3 (column C3, center) in Fig. 3.

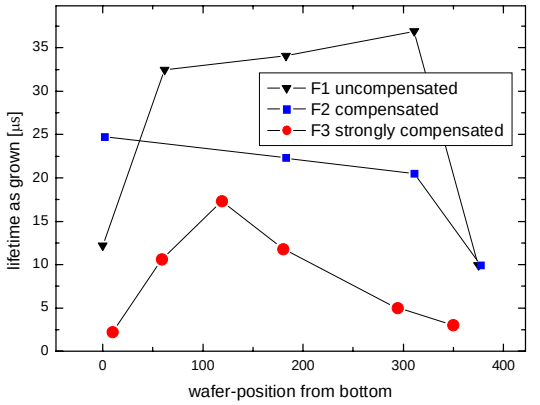


Figure 3: Lifetime of ingot F1, F2 and F3. The points indicate the averaged values over the whole area of the 156x156mm ^{2} wafers - the lines serve only as guides to the eye.

It can been seen clearly, that the lifetime of the wafers in the as grown state decreases with increasing level of compensation. However, often the as grown lifetime of Si wafers is not strictly related to the solar cell efficiencies obtainable using the respective material as it can be significantly improved during the solar cell process. As it is well known, that the most important improvement arises from the gettering effect of a phosphorous diffusion, wafers from ingot F3 have been subjected to a P-diffusion step. The lifetime has been measured after removal of the diffused regions and subsequent coating of the wafers by PECVD-SiN_x. These measurements and the values measured on neighbouring as-grown wafers are shown in Fig. 4 for two bricks of ingot F3.

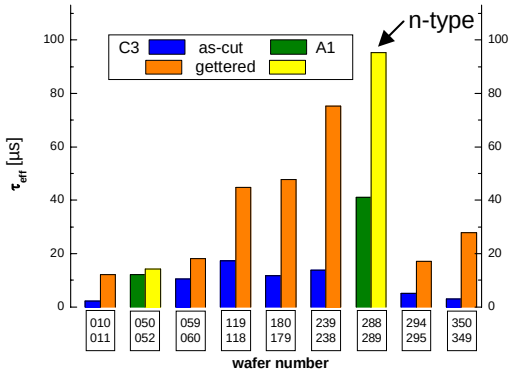


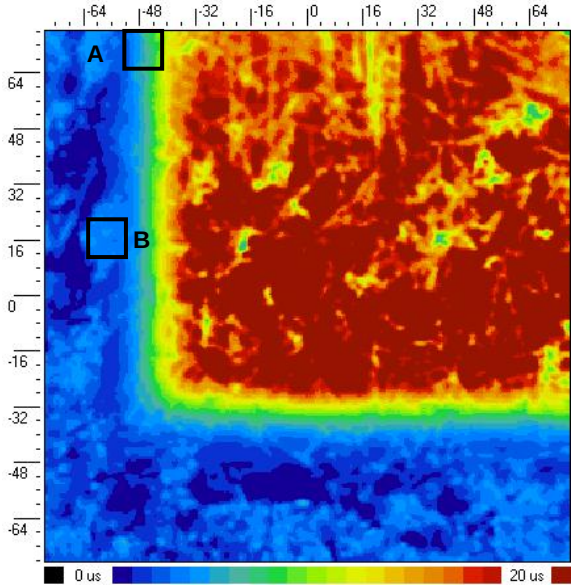
Figure 4: Lifetime of as-grown and P-gettered wafers from ingot F3 column C3 (center of the ingot) and column A1 (corner). Note that the wafers 288 and 289 from column A1 are n-type, all wafers from column C3 are p-type.

All lifetime values presented in this section are values averaged over entire wafers (156x156 mm^2). The diffusion lengths have been calculated using PC1D [7] from the lifetimes supposing ideal carrier diffusivities/mobilities. As this supposition applies not for mc-Si (see section 4), the calculated diffusion lengths are not exact (but too high) but make it at least possible to compare p- and n-type-Si.

The gettering experiment shows that even the regions with the strongest compensation (wafer 349 (p-type) in column C3 and 289 (n-type) in column A1) feature high lifetimes after P-gettering: τ = 30 μs ($L_{diff} \approx$ 320 μm) and τ = 95 μs ($L_{diff} \approx$ 336 μm) respectively. These lifetimes, which can certainly be further increased by a hydrogen-passivation occurring e.g. during a SiN_x-coating during the cell process, enable the fabrication of thin (< 200 μm) solar cells with efficiencies similar to standard industrial solar cells. Gettering experiments of this type for ingot F1 (uncompensated) and F2 (moderately compensated) are under preparation and will be presented in a future publication. The resulting lifetimes after gettering are expected to be at least as high as for ingot F3. At least from this point of view, compensation seems not to have a strong negative effect on the carrier lifetime.

As one expects for mc-Si, the local resolved mappings shown in Fig. 5 reveal a large inhomogeneity.

a) F3-A1-50



b) F3-A1-52

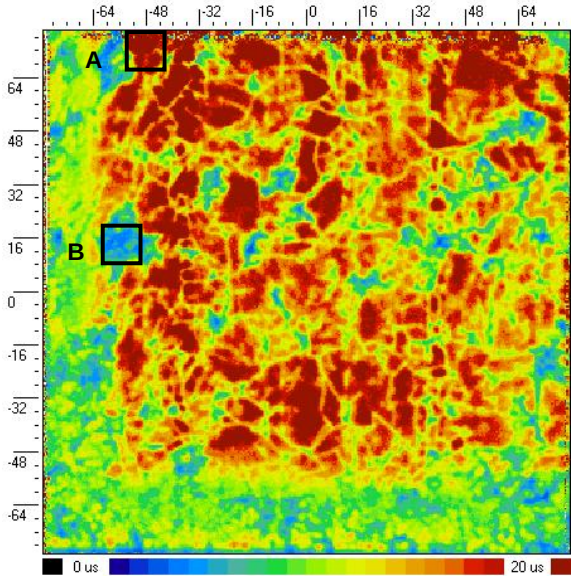


Figure 5: a) as grown lifetime of wafer #50 and b) lifetime of P-gettered wafer #52 from column A1 from the corner of ingot F3. The low-lifetime region caused by outdiffusion of impurities from the crucible is clearly visible on the lower edge and on the left of wafer #50.

Besides the inhomogeneity within the wafers, also the response to P-gettering of different regions of the wafers shows large differences. The detailed characterization of regions in which the lifetime is strongly increased by P-gettering and the identification of defects which impede such an increase could deliver useful information for optimization of the production process of mc-Si ingots. To have a closer look at these effects, 1x1 cm^2 samples have been cut out from the wafer 50 and 52. While the lifetime in sample A shows a large increase after P-gettering, sample B seems to remain nearly unchanged. These samples have been characterized using the Electron Beam Induced Current technique (EBIC). The results are reported in the following section.

3 DEFECT STUDY BY EBIC

Electron Beam Induced Current (EBIC) measurements at temperatures between room temperature (290K) and 90K (using a cryostage cooled by liquid nitrogen) were carried out on selected samples using a Vega TS5136 XM Tescan Scanning Electron Microscope (SEM) equipped with an EBIC apparatus. The acceleration voltage of the SEM was fixed at 25 kV and the beam current was kept below 10 pA. The surface of the 1x1 cm^2 samples has been mechanically polished. To ensure the cleanliness of the surface, the samples have been subsequently dipped for a few seconds in an acidic Si-etch (HF, HNO_3, acetic acid). In order to create a carrier collecting Schottky-diode, a 20 to 30 nm thick layer of Al (for the p-type Si-samples) or Au (for the n-type samples) has been deposited by thermal evaporation on a 5x5 mm^2 area using a shadowing mask.

3.1 EBIC study of p-type mc-Si samples from ingot F3

EBIC-measurements at room temperature and at low temperature (90K) have been performed on the samples presented in Fig. 5. The temperature dependence of the EBIC-contrast of a given defect has been explained by Kittler [8]. Following this theory, defects which are heavily contaminated with metal impurities, show a high contrast in the EBIC-picture already at room-temperature. In contrast to that, defects which are lightly or moderately decorated become visible only in EBIC-scans performed at low temperatures.

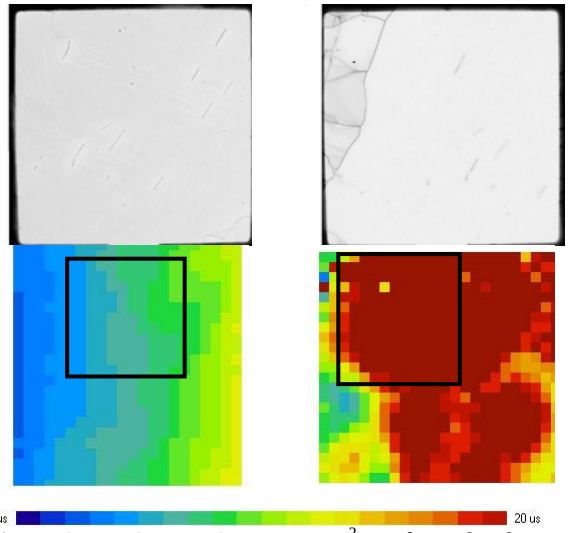


Figure 6: EBIC-scans (top, 5x5 mm^2) performed at low temperature (90K) of the as-grown sample (50A, upper left) and the P-gettered sample (52A, upper right) both from ingot F3, column A1. The corresponding sections of the lifetime-maps (10x10 mm^2) are shown on the bottom. The black frames indicate the relative position of the diode – and thus of the EBIC-scan – within the sample. Note, that the diode on 52A is laterally shifted to the left with respect to that on 50A.

The EBIC scans performed at low temperature (90K) reported in Fig. 6 show a low density of active grain boundaries. The EBIC-scan on 52A is shifted laterally towards the low-lifetime region on the left and therefore shows a small area containing active grain boundaries (GBs) (left of EBIC-scan 52A). The remaining areas of

both samples contain nearly no GBs or only GBs which do not accumulate (getter) impurities. Around the few active GBs in 50A, brighter areas (halos) are visible, indicating an internal gettering effect of these GBs. In the EBIC-scan of 52A these halos disappeared and the whole remaining area appears brighter which shows that most of the impurities have been (externally) gettered through the effect of the P-diffusion. This observation is confirmed by the increase of the lifetime from 7µs (as grown, $L_{Diff} \approx 146$ µm) to 20 µs ($L_{Diff} \approx 246$ µm) after P-gettering (averaged over the whole 1x1 cm^2 sample respectively) and shows, that a region with a low defect concentration can be efficiently cleaned and improved by P-gettering. In contrast to that, the measurements on the samples 50B and 52B show a completely different situation (Fig. 7).

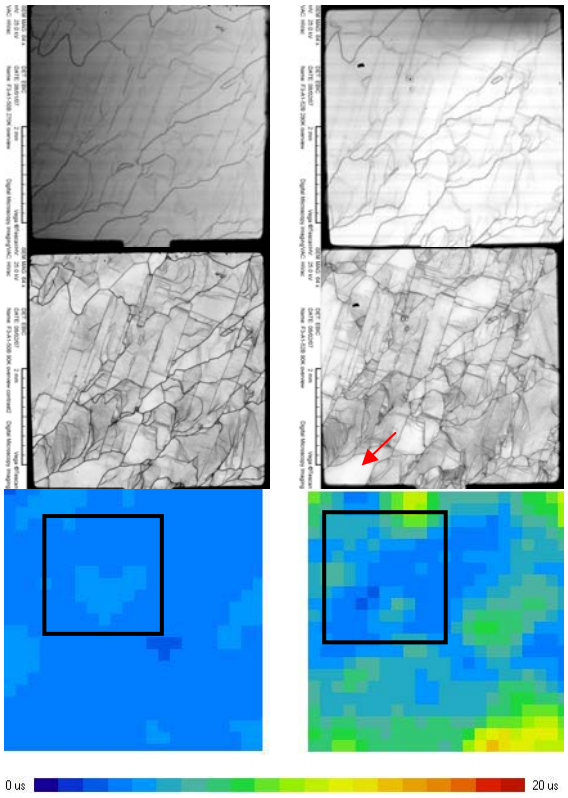


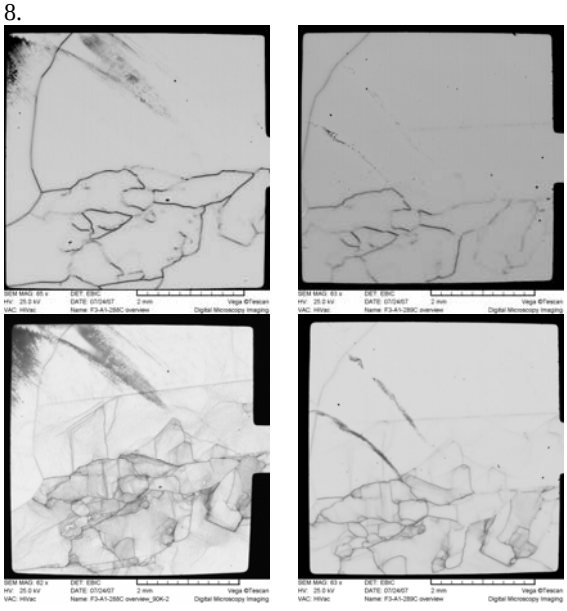
Figure 7: EBIC- and lifetime scans of sample 50B and 52B (ingot F3, column A1). The geometry of samples and diodes is identical to that of 50A and 52A described above. The EBIC-measurements at room-temperature are shown in the upper row, those at low temperature (90K) in the middle. The lowest row shows the relative position of the diodes (EBIC-scans) with respect to the lifetime-measurements (as-grown: 3.7 µs, $L_{Diff} \approx 106$ µm, P-gettered: 6 µs, $L_{Diff} \approx 135$ µm).

A high density of active grain boundaries is visible in the complete zone of the EBIC-scan performed at room-temperature on the as-grown sample 50B (Fig. 7). The measurement at low temperature (90K) reveals that the intragrain regions of these small-grained region are covered completely by a network of dislocations which are lightly decorated with impurities. After gettering, the situation remains nearly unchanged – with exception to single grains in which the impurities have been removed – one of them is marked by the red arrow in Fig. 7. The low lifetime after P-gettering confirms, that this defect-rich zone of the wafer can not be significantly improved by P-gettering. One explanation, beside the small grain size, could be, that during the gettering – which represents a high temperature step - impurities are outdiffusing from the highly decorated dislocations and GBs into the intragrain regions and thus preventing a cleaning and enhancement of the lifetime in these zones. In this case, the gettering effect could possibly be enhanced by specially adapted process parameters (e.g. long diffusion time at moderate temperature) to limit the outdiffusion from the defects while cleaning more efficiently the intragrain-regions. Another reason of the small increase of the lifetime after gettering could be the fact, that this sample originates from the edge region of the ingot (Fig 5. a)) in which the diffusion from SiN_x-particles from the crucible into the Si-bulk causes the creation of SiN_x-precipitates which can neither be gettered by P-diffusion nor passivated by H-passivation [9].

3.2 Study of n-type mc-Si samples

In the case of standard mc-Si, a comparison between p- and n-type material is always difficult, as - due to variations of the processing conditions and used feedstock - each mc-Si ingot differs from another. A look at the resistivity profile of column A1 from ingot F3 in Fig. 2 reveals the possibility of comparing p- and n-type material originating from the same column having comparable resistivities. An important limitation of this comparison is that, originating from the upper part of the ingot, due to segregation effects, the n-type sample features a higher level of compensation and probably a higher contamination with impurities.

A study of the same type as described above for the wafers 50 and 52 (e.g. F3-A1-50B, $\rho \approx 2.9$ Ωcm, $N_A = 4.9 \cdot 10^{15}$ cm^{-3}) has been performed on samples from the wafers 288 and 289 which are n-type and have a comparable net doping level (288C: $\rho \approx 1.3$ Ωcm, $N_D = 3.8 \cdot 10^{15}$ cm^{-3}). The results of the EBIC-measurements and the corresponding lifetime-maps are reported in Fig. 8.



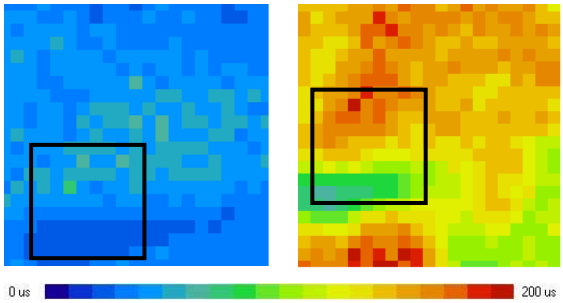


Figure 8: EBIC- and lifetime scans of the n-type mc-Si samples 288C (on the left, as-grown, τ = 42 µs) and 289C (on the right, P-gettered, τ = 147 µs) taken from two neighbouring wafers of ingot F3 (column A1). The EBIC-scans performed at room temperature are shown in the upper row, EBIC at 90K in the middle and the lifetime-scans with the relative position of the EBIC-scans at the bottom.

The EBIC-scan of sample 288C at room temperature shows a large area with very few active defects in the upper half of the sample whereas in the lower half active GBs with high EBIC contrast (up to 25%) can be seen. The EBIC-measurement of the as grown sample 288C at low temperature (90K) reveals in addition a dense dislocation network in the lower half, the upper half still showing a lower density of active defects. The lifetime of the as-grown sample 288C is quite homogeneous and rather low (τ = 42 µs, $L_{Diff} \approx$ 216 µm). After P-gettering the contrast of most of the GBs is diminished (EBIC at room-temperature on sample 289C, Fig. 8) and also parts of the dislocation network disappeared (EBIC at 90K of 289C, Fig. 8). The removal of impurities leads to a strong increase of the lifetime in the defect-free area (upper half of 289C) and to a moderate increase of the area containing active GB (lower half). The average lifetime of the 1x1cm^2 sample is increased to 147 µs ($L_{Diff} \approx$ 415 µm).

4 HALL MEASUREMENTS

The influence of gettering steps on the mobility of the majority charge carriers and an eventual correlation between mobility and minority carrier lifetime is another interesting question. In order to answer to this, Hall measurements at room-temperature, using a magnetic field of 0.5 T, have been performed on samples from ingot F1, F2, F3. The results of these measurements are summarized in Table I

Table I

a) p-type samples from ingot F1 and F2

Sample	**ρ [Ohm cm]**	**μ_{Hall} [cm^{-2}Vs^{-1}]**
F1-C3-184A	0.95	254
F2-C3-312A	1.1	240

b) p-type samples from ingot F3, as grown and after P-gettering (sample 50B was broken)

Sample F3-		**ρ [Ohmcm]**	**μ_{Hall} [cm^{-2}Vs^{-1}]**	**τ [µs]**
A1-50A	as-g	2.6	260	7
A1-52A	P-diff	2.8	236	20
A1-50C	as-g	2.4	264	0.8
A1-52B	P-diff	2.9	246	6
A1-52C	P-diff	2.3	231	12
A1-50D	as-g	2.5	247	22
A1-52D	P-diff	2.7	218	150

c) n-type samples from ingot F3, as grown and after P-gettering

Sample F3-		**ρ [Ohm/cm]**	**μ_{Hall} [cm^{-2}Vs^{-1}]**	**τ [µs]**
A1-288A	as-g	4.4	580	51
A1-289A	P-diff	4.5	591	136
A1-288B	as-g	1.2	801	18
A1-289B	P-diff	1.1	822	69
A1-288C	as-g	1.3	742	42
A1-289C	P-diff	1.1	818	147

The small variations of the values for the Hall-mobilities μ_{Hall} presented in Table I a) and b) show firstly, that for the p-type mc-Si samples originating from ingot F1, F2 and F3 the level of compensation has no impact on μ_{Hall}. Secondly, samples with very different lifetimes (with or without P-gettering) feature quite similar mobility, which applies also to the n-type samples from ingot F3 (Table I c)). The μ_{Hall} measured on the p-type samples correspond quite well to average values reported for samples from the center of mc p-type Si-ingots by [6] (μ_{Hall} = 255 cm^{-2}Vs^{-1}, uncompensated commercial PV-Si wafer) and [10] (μ_{Hall} = 250 cm^{-2}Vs^{-1}, uncompensated, grown from off-cut Si). This gives an indication, that for the here presented samples, the reduction of μ_{Hall} with respect to the theoretical limit ($\mu_{Hall} \approx$ 440 cm^{-2}Vs^{-1} for ρ=2.5 Ωcm) can be explained by scattering mechanisms commonly occurring in uncompensated mc-Si.

In the case of the n-type samples, the μ_{Hall} seems rather low. Though the values lie fairly below the highest reported values (μ_{Hall} = 1271 cm^{-2}Vs^{-1}, [6]) they exceed those reported for the wafers from the top of an *uncompensated* n-typ mc-Si ingot made from pure electronic-grade feedstock: 448 ≤ μ_{Hall} ≤ 587 cm^{-2}Vs, ρ ≈ 0.4 Ωcm, [6]. Given the fact, that the here studied n-type samples are as well originating from the top region of the ingot (wafer 288 out of 360), compensation seems not to be necessairy to explain the rather low μ_{Hall}. To figure out exactly, if there is a impact of compensation on μ_{Hall}, temperature-dependent Hall measurements of samples with different (high) levels of compensation are necessary to study the scattering mechanisms in more detail. For the moment, a reduction of the mobility by compensation seems not to occur – at least for the compensation levels studied up to now.

5 CONCLUSIONS AND OUTLOOK

The study of three p-type mc-Si ingots with different levels of compensation (one of them resulting partially in n-type) has shown that the carrier lifetime of the as grown material decreases with increasing compensation. However, though being strongly compensated, ingot F3 shows a large improvement by P-gettering, leading to high lifetimes (up to 100µs averaged over an entire 156x156 mm^2, p-type mc-Si wafer). It can be noted that, in spite of the higher impurity concentration and the higher level of compensation, the diffusion lengths of the minority carriers in the P-gettered n-type samples are similar or even higher than those measured in the studied

P-gettered p-type samples.

EBIC-scans at temperatures between room-temperature and 90K have been performed on various (p- and n-type) samples which show – in terms of carrier lifetime - different responses to P-gettering. The correlation of the EBIC- and lifetime-maps illustrates clearly that defect-rich areas are practically not improved by the here applied P-gettering process. At the same time, small-grained areas often have a high density of dislocations in the intragrain regions. In contrast to that, areas with a low defect density and large grains can be cleaned and thus improved significantly by P-gettering. In this respect, no difference between p- and n-type mc-Si has been observed.

The analysis of Hall-measurements at room-temperature shows that neither compensation nor P-gettering has an impact on μ_{Hall}. This applies for p- and n-type mc-Si. From this and from the high lifetimes found in the (strongly compensated) ingot F3 after P-gettering, it can be concluded that – in the range of the levels of compensation studied in the present work - compensation has no negative impact on the electrical characteristics of p- and n-type mc-Si. Thus, compensated Si-material could be used as feedstock for Si-wafer production without a significant reduction in solar cell efficiency. This confirms the conclusions of a theoretical study presented in [11] and of the experimental results from [12]. The high diffusion lengths in the here studied, strongly compensated (and containing a high concentration of impurities) n-type mc-Si confirms again the high potential of n-type mc-Si, particularly for the less pure SoG-Si.

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